Q.P. Code: 19EC4212 **R19**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

M.Tech I Year II Semester Regular Examinations October-2020

ALGORITHMS FOR VLSI DESIGN AUTOMATION

(VLSI)

Time: 3 hours Max. Marks: 60

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1		What are the several purpose methods for combinational optimization? Explain briefly.	**12M**
		OR	
2	**a**	How combinational optimization is achieved using Local and Tabu search?	**6M**
	b	Explain the following: (i) Backtracking. (ii) Branch and bound programming.	**6M**

UNIT-II

3	**a**	What is layout compaction? Explain algorithms for constrained graph compaction.	**6M**
	b	Explain about the important abstraction levels that are necessary for a specific simulation tool.	**6M**
		OR	
4		With suitable examples explain the switch level modeling and simulation.	**12M**

UNIT-III

5		Explain how ROBDD can be used for combinational optimization.	**12M**
		OR	
6	**a**	Draw Binary-Decision diagrams for an Inverter.	**6M**
	b	Write short notes of logic synthesis	**6M**

UNIT-IV

7	**a**	List & explain any two scheduling algorithms.	**6M**
	b	Describe High-level Transformation	**6M**
		OR	
8		Explain the following algorithms	
	a	ASAP algorithm.	**6M**
	b	Mobility based scheduling.	**6M**

UNIT-V

9	**a**	Explain the types of logic blocks for FPGA with neat sketches.	**6M**
	b	Develop a routing algorithm for the Non-segmented model.	**6M**
		OR	
10	**a**	How the routing network is modeled in FPGA?	**6M**
	b	Discuss the routing Algorithm for staggered model and compare it with segmentation model.	**6M**

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